Sub Code: R2331024B **R23** **SET-1**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY-GURUJADA VIZINAGARAM

III B. Tech I Semester Regular Examinations November -2025

Computer Architecture and Organization

(EEE)

Time: 3 hours **Max. Marks: 70**

The Question paper consists of Part A & Part B.

Part A is compulsory, Answer all questions. Part B Answers any one question from each unit.

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1		PART-A	(20Marks)
	a)	Define computer architecture and computer organization.	[2]
	b)	What is instruction format? Give an example.	[2]
	c)	Differentiate between hardwired control and micro-programmed control.	[2]
	d)	Define addressing modes. Mention any two types.	[2]
	e)	What is a pipeline hazard?	[2]
	f)	Define cache memory and explain its purpose.	[2]
	g)	What is interrupt-driven I/O?	[2]
	h)	Explain the concept of virtual memory.	[2]
	i)	What are the advantages of RISC architecture over CISC?	[2]
	j)	Define Flynn's classification of computer architectures.	[2]
		PART-B	(50Marks)
		Unit - I	
2	a)	Explain the functional units of a basic computer with a neat block diagram.	[5]
	b)	Describe the basic computer instructions and their formats	[5]
		(OR)	
3	a)	Explain the instruction cycle and different phases involved in it.	[5]
	b)	Discuss the concept of micro-programmed control unit with block diagram.	[5]
		Unit - II	
4	a)	Explain different types of addressing modes with examples.	[5]
	b)	Describe the design and working of an accumulator-based CPU.	[5]
		(OR)	
5	a)	Explain arithmetic and logic micro-operations with suitable examples	[5]
	b)	Discuss the role of control memory and its organization.	[5]
		Unit - III	
6	a)	Explain the concept of pipelining and its advantages.	[5]
	b)	Discuss different types of pipeline hazards and methods to overcome them.	[5]
		(OR)	
7	a)	Explain instruction-level parallelism and compare it with pipeline processing.	[5]
	b)	Describe vector processing and array processors with suitable examples.	[5]
		Unit - IV	
8	a)	Explain cache memory organization and mapping techniques.	[5]
	b)	Discuss the concept and design of virtual memory.	[5]
		(OR)	
9	a)	Describe the working of associative memory.	[5]
	b)	Explain memory hierarchy with a neat diagram.	[5]
		Unit - V	
10	a)	Explain I/O interface and I/O bus structure	[5]
	b)	Describe asynchronous and synchronous data transfers.	[5]
		(OR)	
11	a)	Explain the characteristics and design principles of RISC architecture	[5]
	b)	Discuss Flynn's classification of computer architectures in detail.	[5]

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